DTMOS IV Efficiency Advantages of Superjunction Transistors

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Summary
Superjunction MOSFETs are able to deliver a combination of high conduction and switching efficiency, small die area and high breakdown voltage that conventional devices cannot achieve. This article explains how superjunction technology delivers these benefits for designers, and examines the latest developments that will enable performance to be further extended in the future.

Introduction: Taking MOSFET Performance to the Limit
Energy efficiency is a top priority for designers targeting applications such as solar inverters, PC adapters, lighting ballasts and power supplies. To minimise the energy lost in the power supply, engineers must consider the loss mechanisms in the main power switch, which may comprise a single MOSFET or a MOSFET bridge depending on the topology.

At the MOSFET silicon level, techniques to reduce the device's on-resistance ($R_{DS(ON)}$) have focused on fabricating smaller cells that allow increased cell density leading to a lower $R_{DS(ON)}$ pin relation to die size. Although a larger die can accommodate more cells, effectively reducing on-resistance, this comes at the expense of greater cost and a larger package size.

Switching losses are reduced by minimising parasitic capacitances around the gate, source and drain, and reducing stored charge in the gate and gate-drain regions ($Q_g$ and $Q_{GD}$). The gate charge ($Q_g$) determines the energy the gate driver must supply to switch the device. A low gate charge allows designers to use high switching frequencies, which permits the use of small external filtering components in order to minimise solution size and cost.

With improvements over several generations, standard MOSFETs are approaching natural limits in terms of minimising $R_{DS(ON)}$ for a given MOSFET voltage rating ($V_{BDSS}$), and improving switching performance by reducing capacitances and gate charge. MOSFETs with a high $V_{BDSS}$ of around 500V or higher are often needed to ensure adequate safety margin in mains-voltage applications. In devices such as these, the dimensions and doping of the drift
region – which is the most important region governing the device on-resistance - must be tightly controlled to achieve the desired $V_{\text{BDSS}}$. In practice, there is a natural limit, termed the silicon limit, beyond which the MOSFET’s on-resistance for a given die area cannot be reduced without also reducing breakdown voltage. There are also practical limits to improvements in switching performance. For a given MOSFET technology, measures taken to reduce the on-resistance tend to increase the gate charge, hence forcing a compromise between conduction and switching performance.

**Superjunction MOSFETs**

Superjunction MOSFET technology has a fundamentally different structure that breaks through these limitations. Rich doping of the N region reduces resistivity, resulting in significantly lower on-resistance than is possible in a conventional MOSFET. To achieve the desired breakdown voltage, this region is bounded by adjacent deep P-type trenches. This produces a column structure as shown in figure 1b, compared to the conventional MOSFET structure illustrated in figure 1a.

![Conventional MOSFET Structure (a) and Basic Superjunction MOSFET Structure (b)](image)

Figure 1: Conventional MOSFET Structure (a) and Basic Superjunction MOSFET Structure (b)

Superjunction MOSFETs have been available for a number of product generations. Evolution has delivered improvements in on-state resistance by reducing the pitch and increasing the aspect ratio of the P- and N-type columns. Multi-axial processes have proved...
successful in producing columns of close pitch and high aspect ratio. This approach utilises repeated stages of ion implantation and buried n-type epitaxial growth.

Toshiba has used multi-axial processes in its previous generations of DTMOS superjunction devices. One limitation of this approach is that the number of process steps must be increased to achieve each successive improvement in on-state resistance. This tends to increase production cost. A new technique is required to further this path of development, fabricating columns at closer pitch and higher aspect ratio, in order to deliver cost-effective devices offering even better on-state resistance than the previous generation.

**Further Improvement of Superjunction MOSFETs**

Deep trench filling is a new technique designed to enable future generations of superjunction MOSFETs to support further efficiency improvement. The process comprises deep trench etching followed by P-type epitaxial growth, eliminating a large number of process steps and so providing a cost-effective route to improving on-state resistance. Figure 2 compares the profile of the P-type trench achievable using deep trench filling, with that produced by the multi-epitaxial process.

![Figure 2a. Superjunction Structures](image-url)
Toshiba has used deep trench filling in its DTMOS IV superjunction process. This has allowed closer trench pitch compared to the DTMOS III (multi-epitaxial) process, ultimately yielding 30% better on-state resistance per die area (specific on-resistance). DTMOS IV MOSFETs claim the lowest specific on-resistance in the entire 600V class, and deliver the lowest $R_{DS(ON)}$ among competing devices in each power-package type. Beside the pure improvement of Ron vs chip size, the important parameter – thermal dependency of $R_{DS(ON)}$ – is significantly lower at DTMOS IV, compared to the competition and the previous generation. Due to this, efficiency of operation at higher temperatures can be improved.
Figure 3. Thermal dependency of $R_{\text{DS(ON)}}$

**Switching and Noise Performance**

Although narrowing the column pitch holds the key to minimising on-resistance without increasing die size, it also has the effect of reducing the gate charge, $Q_G$. Care must be taken to avoid excessive reduction of $Q_G$, as this can allow high $dV_{DS}/dt$ when switching leading to an increase in emission of electromagnetic interference (EMI). On the other hand, a low value of $Q_G$ helps to reduce losses in the gate-driving circuitry, and also allows designers to specify a lower-output gate-driving device and thereby save system cost and size. DTMOS IV has an optimised gate structure designed to achieve $R_{\text{DS(ON)}} \times Q_G$ and $R_{\text{DS(ON)}} \times Q_{GD}$ figures of merit comparable to those of the preceding DTMOS III generation.

Another aspect to consider in the design of Deep Trench superjunction transistors is the effect on device output capacitance of doping in the N and P regions. High doping levels tend to increase output capacitance, which impairs power supply efficiency under light-load conditions. DTMOS IV devices have 12% lower output capacitance than the previous generation, by virtue of smaller die size, and have the lowest output capacitance among comparable devices on the market.

**Smaller die size - Extra Package Options**

By enabling the on-resistance per die square millimetre – also known as specific on-resistance – to be reduced significantly below the silicon limit for standard MOSFETs,
DTMOS IV superjunction technology enables devices to offer lower on-resistance using the same package styles as earlier devices. Alternatively devices can be offered in smaller packages, such as surface-mount power packages, giving greater flexibility for power supply designers to optimise energy efficiency and power density.

DTMOS IV devices can be offered in an expanded range of industry-standard packages, comprising DPAK, IPAK, D2PAK, I2PAK, TO-220, TO-220SIS, TO-247, TO-3P(N) and TO-3P(L). The largest of these packages, the TO-3P(L), allows the lowest $R_{\text{DS(ON)}}$ at 0.018Ω. At the other end of the spectrum, the smallest DTMOS IV item offers a 600V device in the DPAK package, with $R_{\text{DS(ON)}}$ down to 0.34Ω.

Fully isolated TO-220SIS package solutions, using Toshiba’s established copper connector technology, will offer the finest split of $R_{\text{DS(on)}}$ from 0.9Ω to the best in class performance of 0.065Ω, in this form factor.

D2PAK and I2PAK packages are often chosen for applications such as solar micro inverters, where 600V fourth-generation superjunction MOSFETs can offer $R_{\text{DS(ON)}}$ from 0.19Ω to 0.16Ω. For mainstream industrial solutions TO-220 solutions have $R_{\text{DS(ON)}}$ ratings ranging from 0.38Ω to 0.088Ω.

**The next DTMOS generation**

The deep trench filling process enables device designers to further extend the advantage of superjunction MOSFETs, in terms of specific on-resistance, by creating deeper, narrower P-type trenches and enhancing control over trench shape and uniformity.

Continued improvement, by enhancing process control and achieving even more favourable trench dimensions, should allow further reduction of device on-resistance even at high voltage ratings above 600V, as well as the integration of high speed diodes.

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