How to handle the increasing ECC requirements of the latest NAND Flash memories in your Industrial Design

By Toshiba Electronics Europe

Overview

As NAND Flash memory moves towards more advanced process nodes, the cost of devices is reduced but the cells become more vulnerable to program/erase stresses. The new technology requires more Error Correction Code (ECC). Unfortunately, many chipsets or controllers are unable to perform more than 1-bit or 4-bit ECC. BENAND™, an SLC-NAND with internal ECC, takes this challenge from the controller. This paper describes how BENAND can be smoothly integrated into industrial and other applications.

Introduction:

NAND Flash is used in a wide variety of industrial, communication, automotive and consumer devices requiring non-volatile storage for code, data or content. To respond to market demands for lower costs and increased storage capacity, fabrication technology is advancing quickly to each successive new process node. This strategy is successful in achieving the small die sizes and high memory densities needed to satisfy market demand.

With every gain there typically comes a challenge, however. In the case of deep nanometre NAND Flash, smaller process geometries bring demands for increased error-code correction. This is necessary to guarantee reliability in line with engineers’ expectations.

As with standard NAND Flash, regardless of process geometry, issues such as high-voltage stress during program/erase cycles can alter or damage individual cells. Over time the number of affected cells increases. The only way to manage this gradual deterioration is to perform error correction on all data read from the device and to avoid using known affected cells. At smaller process nodes, the individual cells are more susceptible to failure induced by high-voltage stress.
To date, more error correction has been needed for Multi-Level Cell (MLC) NAND technology, while Single-Level Cell (SLC) NAND has typically required only 1-bit ECC for densities up to 4Gb fabricated at 43nm. A 1-bit ECC algorithm is defined as being able to correct one failure bit per 512 bytes. The latest SLC NAND Flash devices, fabricated at 32nm or 24nm, require 4-bit or 8-bit ECC, respectively, per 512 bytes. Figure 1a and 1b contrast the cost-down advantages of advanced process technologies with the associated increases in ECC complexity.

For many existing applications that use SLC NAND memory, such as industrial designs, communication processors and automotive systems, the 1-bit ECC is implemented in the host with no significant effect on application performance. Migrating to ‘cutting-edge’ memories that require 4- or 8-bit ECC significantly increases demand on the processor. In embedded applications generally, spare processing capability can be so limited as to prevent handling the increased error-correction demand in software. As a result, migrating to the latest NAND technologies typically calls for hardware-based ECC.

BENAND Versus Standard SLC

Recently, in the case of the latest SLC NAND solutions, a new option has become available to the designer, namely BENAND™ (Built-in ECC NAND) memory, which features an embedded ECC function.

As figure 2 illustrates, BENAND removes the burden of ECC from the host processor without requiring an additional hardware controller. It is important to note that BENAND uses the common NAND interface, thereby ensuring compatibility with general SLC NAND Flash in areas such as command set, device operation, packaging and pin configuration. As
indicated in figure 2, issues such as bad-block management and wear levelling are handled in the same way as with raw SLC NAND.

BENAND technology allows OEMs to benefit from the reduced cost and increased memory density associated with smaller process geometries, whether in completely new designs or when migrating existing applications to more advanced memory solutions. An existing design can be migrated without changing established hardware.

Figure 2: Comparison of BENAND and Raw SLC NAND.

The BENAND ECC stores results generated by checking the data read out of memory in a spare area, in the same way that spare area is utilised in a standard SLC NAND. Figure 3 illustrates how the ECC for a 2Kbyte page requires 64 bytes of spare area. The BENAND ECC also checks for errors in data from the spare area, to prevent damaged cells from causing incorrect results.
Performance Comparison
The effective speed of BENAND is comparable to that of raw SLC NAND. Although BENAND in fact has longer read (tR) and program (tPROG) times, due to the internal ECC, the host-side ECC needed for raw SLC will add the same - or longer - delay.

In normal operation, the BENAND always delivers valid data, containing zero errors due to failed memory cells. The system is normally unaware of the physical condition of the NAND cells. Sending a Status Read command causes the BENAND to report if a page contains corrected or incorrectable cells. Checking the memory using Status Read is recommended, to safeguard long-term reliability of the application.

It is true that NAND controller ICs capable of supporting higher than 1-bit ECC/512Byte for memories below 43nm are on the market today. These can allow raw SLC NAND to be used instead of BENAND. However, the efficiency of the ECC algorithm is critical if the system is to avoid read failures. If the controller cannot support 8-bit ECC/512Byte for 24nm Flash, BENAND can offer an ideal solution.

BENAND, with its built-in ECC, is able to maintain reliability comparable to that of a raw SLC NAND fabricated at the same process node and using ECC performed in the host.

Design-in and Compatibility
If BENAND is used to replace a standard SLC NAND in an existing application, best performance can be achieved by disabling any ECC performed by the host. If host ECC cannot be turned off, the BENAND will continue to provide error-free operation using its own built-in ECC.

A common question from developers relates to the availability of a second source, particularly when a new category of devices is revealed. Toshiba’s BENAND is functionally...
compatible with SLC devices from alternative vendors, and requires limited modification of commands to use one device type or the other. Additionally, the BENAND supports the Status Read command.

Toshiba BENAND devices are packaged as standard TSOP-I-48-P and 63-ball BGA devices, which are pin compatible with known SLC packages. In addition, Toshiba offers a very small 6.5mm x 8.0mm 67-ball BGA version. This is ideal for use in new designs for extremely space-constrained applications.

**Coming Soon**
A number of BENAND Flash memories by Toshiba are already in the market. Next-generation devices fabricated using the latest 24nm process technology, featuring built-in 8-bit ECC, will soon be introduced in 1Gbit and 2Gbit densities.

Further information may be found in the question and answer sheet on the Toshiba web site (see link below).
For more product information visit http://www.toshiba-components.com/memory/benand.html or our Toshiba Electronics Europe's web site at www.toshiba-components.com

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