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White Paper

About MicroTCA.4:

An High-Performance Architecture with I/O and Signal Conditioning Provisions

MicroTCA is a powerful, compact open-standard COTS architecture used in Military, Aerospace, Communications/ Networking, and other industries. By adding rear I/O capability and signal conditioning provisions in the MicroTCA.4 specification, the technology became ideally suited for the High Energy Physics market. This paper will review the MicroTCA.4 background, hardware ecosystem, and latest design advancements.

MicroTCA Background

The MicroTCA (µTCA) open-standard architecture provides a dense, high-speed, managed technology with built-in high availability options. Designed with the High Energy Physics (HEP) community in mind, the MicroTCA.4 sub-specification adds functionality in the provision of µRTMs for signal conditioning and I/O. This makes it attractive for I/O-intensive applications and those requiring mixed-signal capabilities in a single chassis.

A µTCA.4 chassis platform can include the following characteristics:

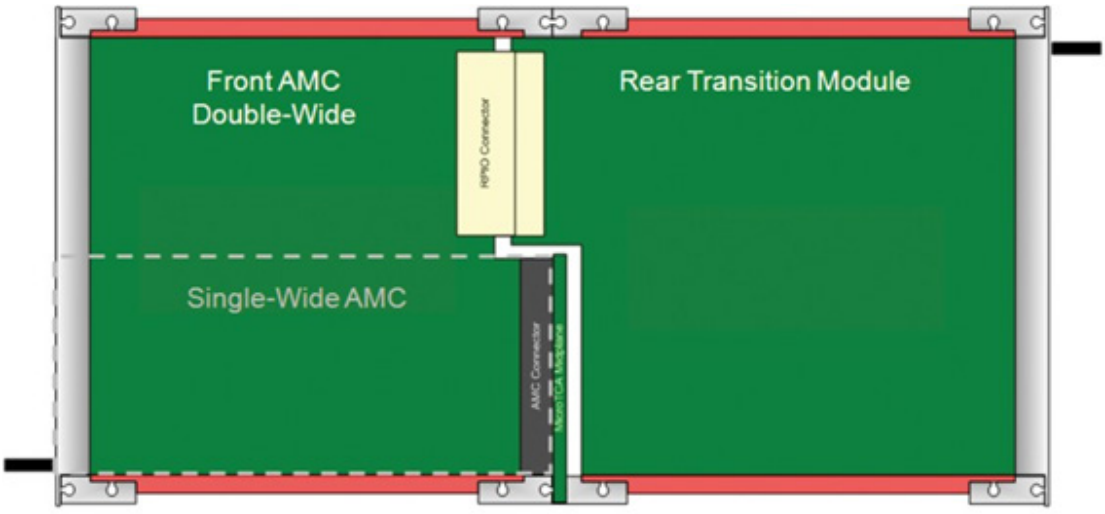
- High reliability chassis with full redundancy of power, cooling and MCH.
- Up to 12 AMC slots, each supporting a micro RTM (µRTM)
- Capability to accept, filter and process many sensor inputs at high data rates.
- Precision clock and trigger generation and distribution
- Compatible with an extensive range of processing and I/O AMCs (since a µTCA.4 chassis is also compatible with standard µTCA.0 AMCs).
- Options for horizontal-mount chassis, may or may not have full redundancy

There are clear advantages to using an open standard COTS architecture that has a firmly established foothold in multiple markets (military, communications, aerospace, networking, etc.)

Mechanical

MicroTCA standardly has approximately 75mm boards in the single module size and approximately 150mm boards in the double module size. MicroTCA.4 uses the double modules and adds an µRTM connector for rear I/O. Figure 1 shows the interface between the front AMC and Rear Transition Module.

Figure 1

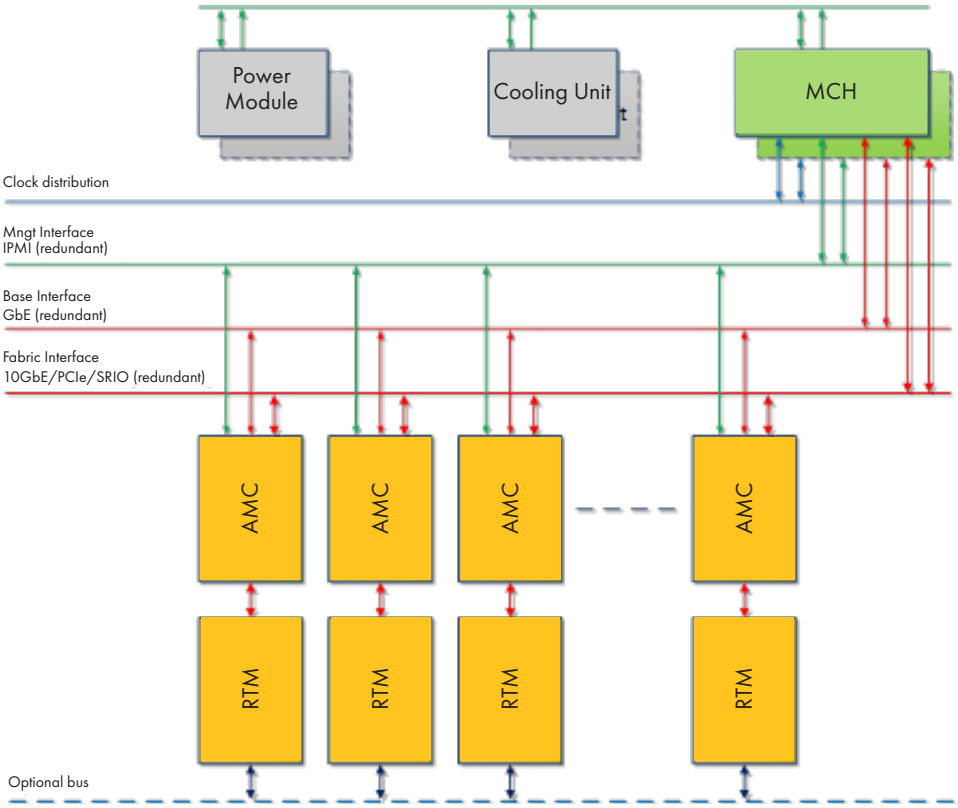


The front module is standard and fully compatible with µTCA.0 with a connector on the rear to connect with the µRTM. The µRTMs are application-specific and need to have pinouts that are compatible with the front board they are plugged into.

System Management

MicroTCA utilizes the platform management of its sister specification, AdvancedTCA. The inherent shelf management of MTCA provides several benefits including failover if a PSU goes out, alarm signals for various levels of system conditions, fan speed control, and more. For example, if a fan goes out, the MCH can be programmed to send a remote signal for repair and speed up the fans in the rest of that section of the chassis until the unit is repaired. In Figure 2 below is a basic conceptual overview of the MicroTCA.4 architecture.

Figure 2



The MCH includes full platform management capability, ensuring all payload AMCs and µRTMs are completely compatible before completing system initialization

Chassis Platforms for MicroTCA.4

The MicroTCA.4 chassis platforms can offer full redundancy, including dual fan trays, dual MicroTCA Carrier Hub (MCH) slots, and up to 4 Power Module (PM) slots. The types of AMCs include high speed FPGA-based ADC and DAC (analog/digital converters and digital/analog converters), data processing modules, Intel-based processors, FMC carriers, and more.

The vertical chassis is typically 8U-9U high, holding up to 12 AMCs and µRTMs in the 19" rack. For redundancy, they typically have 2 MCHs and 2-4 power modules. See Figure 3 for an example.

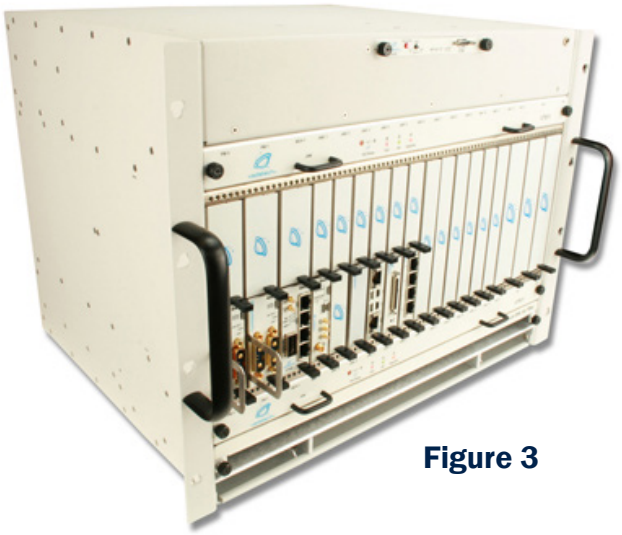


Figure 3

Utilizing an aluminum construction provides a much lighter result while maintaining a strong, reliable frame. Aluminum is a preferred material for some particle physics experiments. The non-ferrous material is critical for the proximity to the magnetic field in these tests. For better cable management, cable ducts can be integrated within the chassis frame below the card cage to protect and route the cables to the rear of the chassis.

VadaTech's fan trays are arranged with sixteen 2" fans each above and below the card cage in a push-pull configuration. The smaller, powerful fans ensure each slot gets optimal airflow, avoiding hot spots. Insertion/extraction of the fan trays is considered as well. By installing easy-glide strips where the fan trays are plugged, they can slide in and out much more smoothly and easily. It is also advisable to utilize shrouded blind-mate connectors for both the male and female ends of the plugs, which prevent damage and ease guided insertion. In addition, the backplane design takes into account the target applications - where precision timing is important - so the clock traces are laid out to give equal track length from MCH to each AMC slot, easing latency equalization.

In a µTCA.4 chassis platform, as on other MicroTCA platforms, the radial I2C bus (IPMI) is routed to each AMC for monitoring/control for each module. A pluggable Telco alarm can be incorporated as well as JTAG Switch Module (JSM) which provides JTAG access to each AMC slot - ideal for FPGA code development. An advantage of the MicroTCA architecture is the ability to utilize multiple fabrics with defined port allocations. Mixed-fabric configurations are supported, either through the Extended Options region or by use of dual MCHs.

Redundant Power Challenges

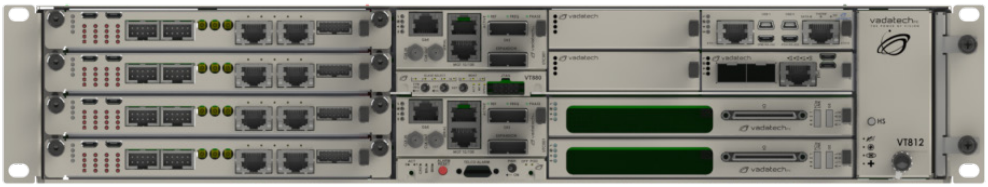
MicroTCA utilizes AC voltage or DC power supplies. The DC voltage range is typically 10-32v or -36v to -75v. The specification has a maximum of approximately 80W/slot. One challenge in MicroTCA.4 systems is to provide significant power in a fully redundant or N+1 mode. By putting the Power Modules on the side of the card cage, you can fit 12 mid-size slots. In the 8U chassis in Figure 4 below, you can have up to 4400W of power with 4x power supplies in an N+1 or 2N mode. Alternatively, the PSUs can be placed below the card cage (adding 1U to the overall height) and have 12 full-sized slots. The Full-size slots are an advantage as you can use a higher density version of the connector for the RTM signals and have more space for a heat sink.

Figure 4

Horizontal Mount Approach

In MicroTCA.4 systems, the chassis is typically vertical-mount to provide the 12 slot maximum. However, not all applications will require all of these slots. It is possible to utilize a horizontal-mount approach to save rack space. In this configuration the cooling orientation would be side-to-side, and the chassis may or may not have redundant cooling. Figure 5 shows a chassis configuration with 4 standard µTCA.0 slots and 4 µTCA.4 slots. This type of design allows the re-use of a wide range of existing single module µTCA.0 boards without the rear I/O connections. It is expected that applications such Mil/Aero, Video Processing, and Energy would find this type of size and configuration attractive.

Figure 5



A/D and D/A Conversion, RF Conversion

In Physics applications, various AMCs are often utilized to down-convert the RF signals and convert analog/digital signals at a very fast sampling rate. For digital conversion, the AMCs are often in the 125- 250 MSPS range for ADC and 250-500 MSPS for DAC. Multi-channel down converters support various frequencies in multiple bands. An example of a MicroTCA.4 10-channel down converter board is shown in Figure 6.

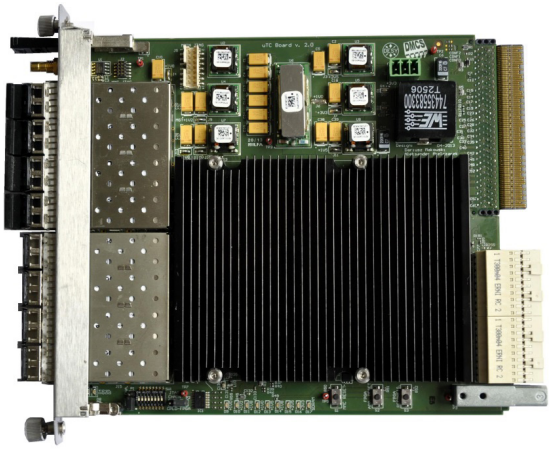


Figure 6

MCH for Higher Speed, Cleaner Signals

The MCH for MicroTCA offers multiple fabric options standard within the specification. This includes PCIe (up to Gen 3), Ethernet (up to 10G), and SRIO (up to Gen 2). An effort for 40GbE speeds is currently in draft in the PCI Industrial Computer Manufacturer's Group (PICMG). Although in draft, many products are already designed to handle these speeds. Figure 7 shows a MCH that supports PCIe Gen3, SRIO Gen 2, 40GbE, and a Crossbar Switch for any protocol to be utilized.

For backplane and front panel clocking, the MCH can provide a low-latency, low-jitter, low-skew M-LVDS clock matrix to ensure the best possible backplane clocking solution. By incorporating a quad PLL clock network synchronizer, the clocks can by synchronized with hitless failover referenced to clocks/pulses coming from the front panel, backplane, on-board GPS/IEEE1588 (PTP)/NTP 1PPS, or SyncE ports. These PLLs can then jitter clean or synthesize arbitrary frequency clocks and pulses to output to the front panel or backplane with up to Stratum-3 holdover criteria.

Figure 7

Beyond Physics Alone

Although MicroTCA.4 was first developed for the High-Energy Physics community, the architecture is suitable for all types of applications where its bandwidth, management/control, I/O, and large ecosystem is an advantage. The AMC/µRTM division was specifically designed to support the combination of off-the-shelf standard processing elements (AMCs) with custom signal conditioning (RTMs), an attractive approach in many industries.